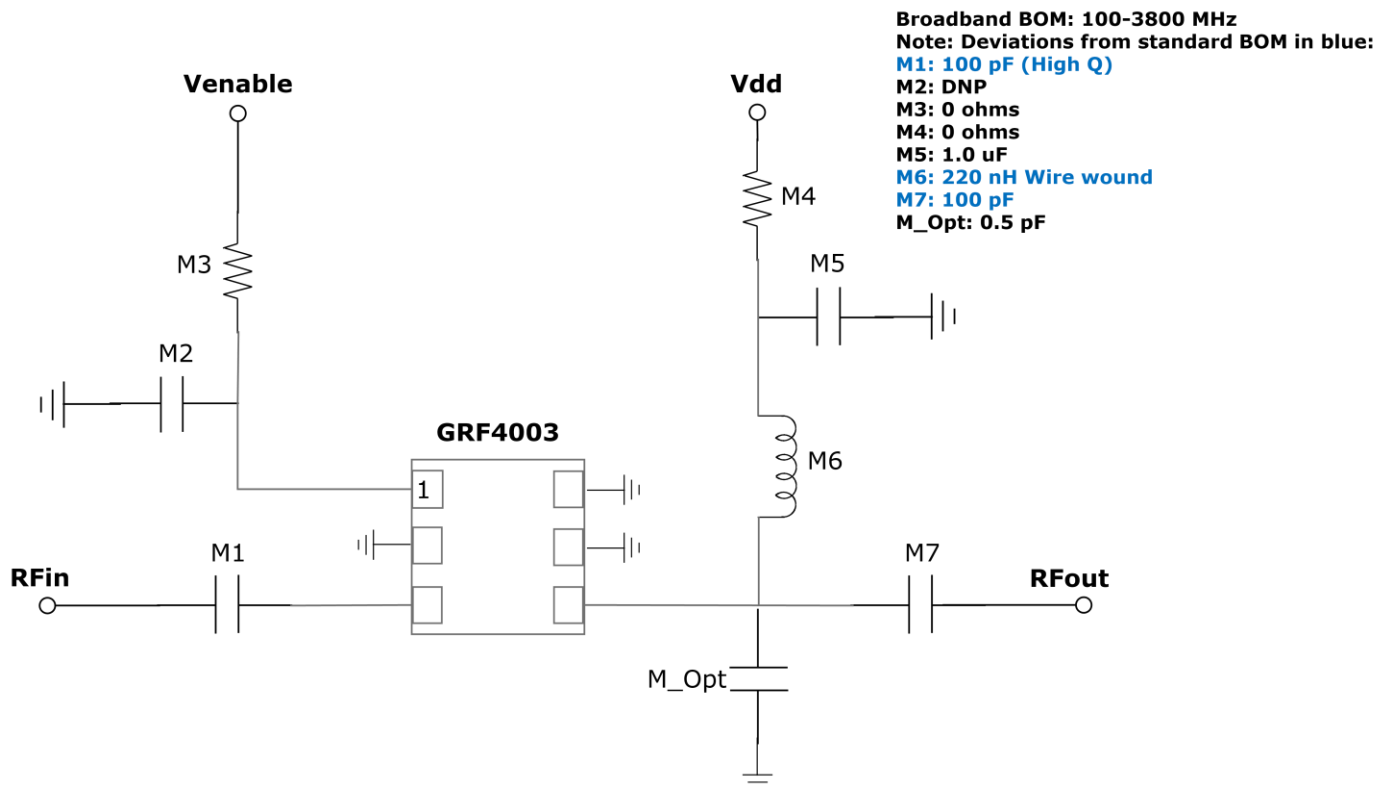


GRF4003 has been developed with the RF system designer in mind. The device offers simple configuration handles which, when adjusted, suit a wide range of applications. The standard evaluation board (EVB) covers frequency range 700 – 3800 MHz. The broadband application discussed herein extends bandwidth down to 100 MHz. Three minor changes to the standard EVB enable the extended bandwidth:





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Two external resistor values are provided for adjusting bias point and enabling trade-offs between the following specifications:

1. Compression Point (IP1dB/OP1dB)
2. Third Order Intercept Point (IIP3/OIP3)
3. EVM (Error Vector Magnitude), which comes as a direct result of 1 and 2 above.
4. Current, and therefore power, dissipated

Bias Point would be defined by supply voltage, drain voltage and drain current.

1. supply voltage, Vdd: system supply, or battery.
2. drain voltage, Vd: that seen at supply pin of device
3. drain current, Idd: current to the device via supply voltage

Desired trade-offs are implemented while maintaining excellent broadband return losses, unconditional stability and sub 1 dB noise figure.

We will demonstrate the broadband application covering frequency range 100 to 3800 MHz, with the intent of obtaining maximum third order output intercept point (OIP3) over frequency. This, combined with sufficient compression point and low noise figure, enable GRF4003 use at multiple points within a radio architecture and across platforms:

1. Linear driver amplifier
2. Final power amplifier (PA) in “small cell” or “picocell” designs requiring 15 – 20 dBm at antenna
3. Low noise amplifier: 1st, 2nd or 3rd stage
4. IF amplifier where up/down conversion between RF and IF is implemented

Thus, GRF4003 offers the convenience of re-use with common board layout and component values.



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The following bias points will be used:

1. $V_{dd} = 2.7/3.0/3.3$ V. Reasoning here explained via discussion of GRF4003 flexibility, which allows for operation over V_{dd}/V_d ranging from 1.8 to 5.0 V (refer to GRF4003 data sheet). With maximum IP3 performance desired over the full frequency range under consideration, $V_{dd}/V_d = 3.0$ V is near optimal. “ V_{dd}/V_d ” used here, as supply and device pin voltage are nearly the same. Viewing the schematic, they are only separated by 3 ohm resistance of the 220 nH choke inductor. In the case where equivalent performance is desired using larger V_{dd} (5.0 V for instance), resistor R2 can be adjusted to reduce device voltage V_d ; and of course, outside the scope of this application note, compression point can be increased by operating with higher V_{dd}/V_d (using lower value at R2).
2. $V_{en} = 1.1$ V. This in the presence of $R1 = 0$ ohm. Likewise, V_{en} can be scaled for a larger supply voltage using the appropriate R1 value.
3. $I_{ddq} = 68/71/73$ mA respectively, resulting from bias voltages above. This current is sufficient in maintaining best linearity (IP3) over frequency and temperature (refer to GRF4003 data sheet for data vs. temperature).

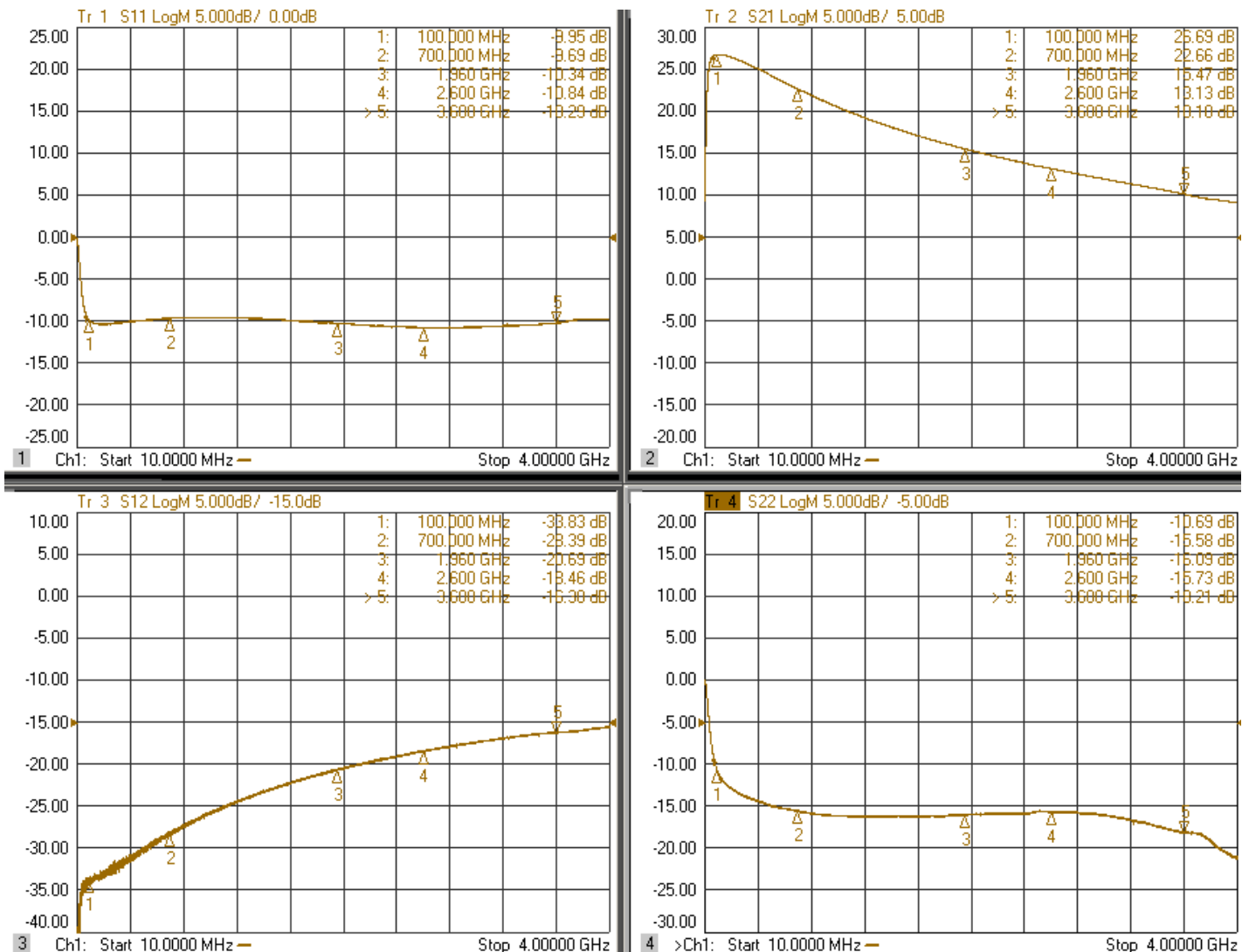


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Resultant data from our optimized broadband application circuit. All reported data taken at temperature = 25C.

Evaluation board s-parameters:

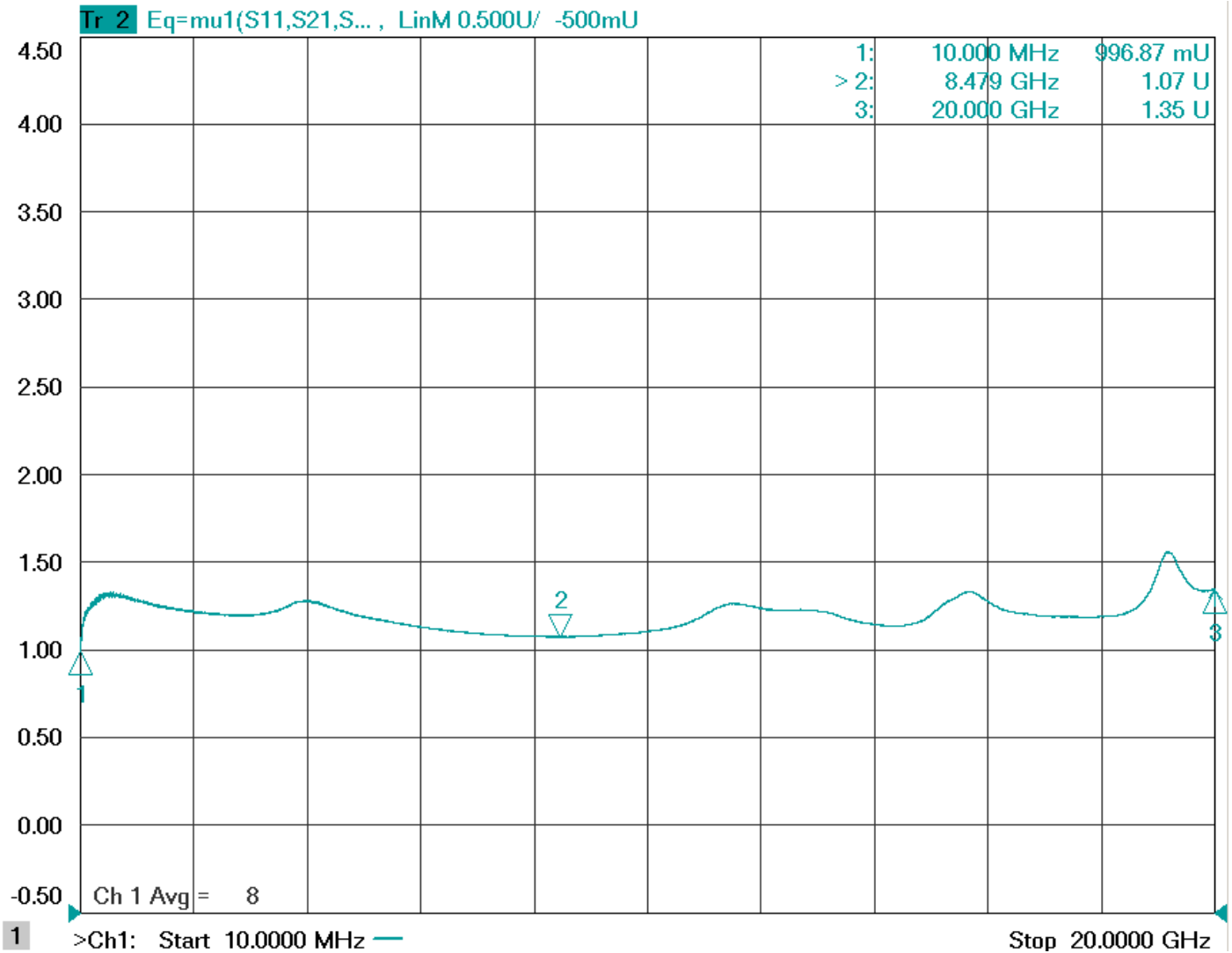




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Evaluation board stability Mu factor:

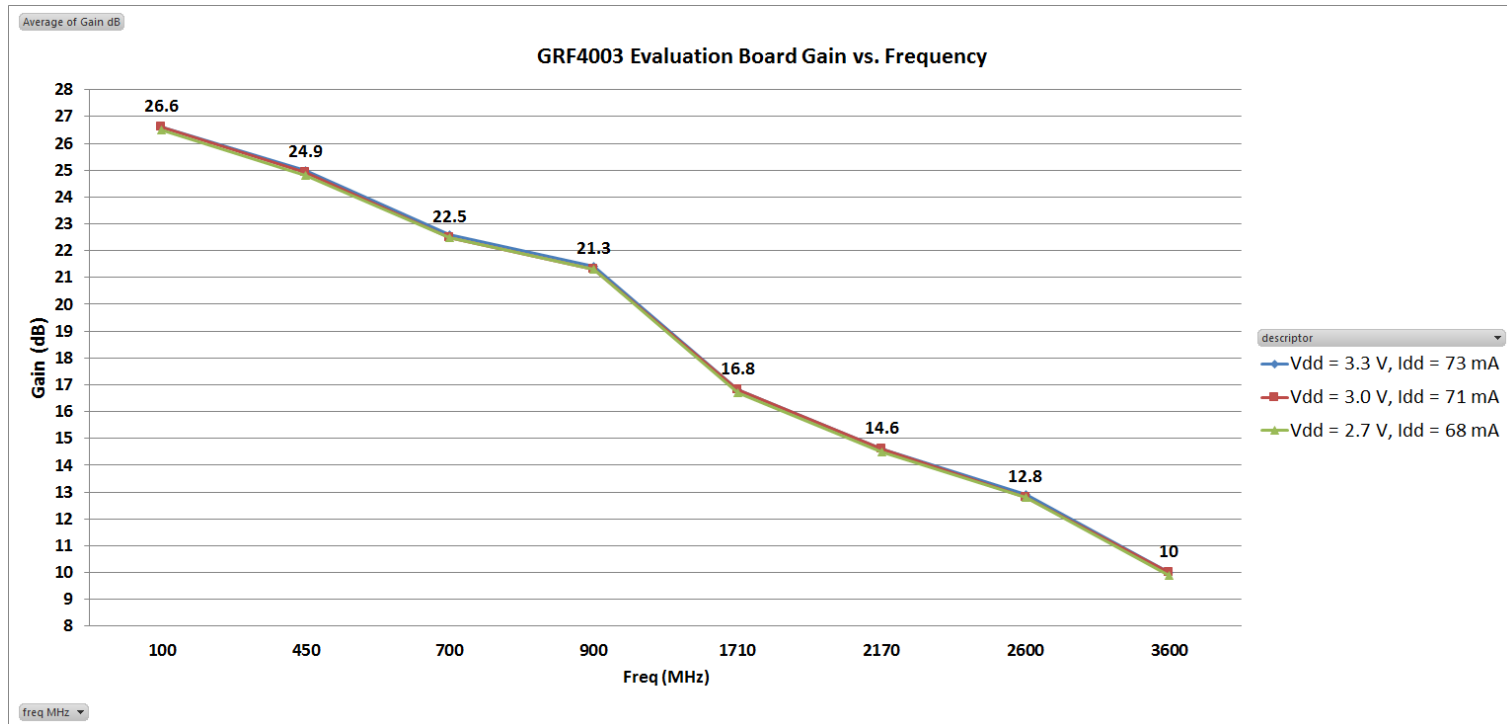




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Gain:

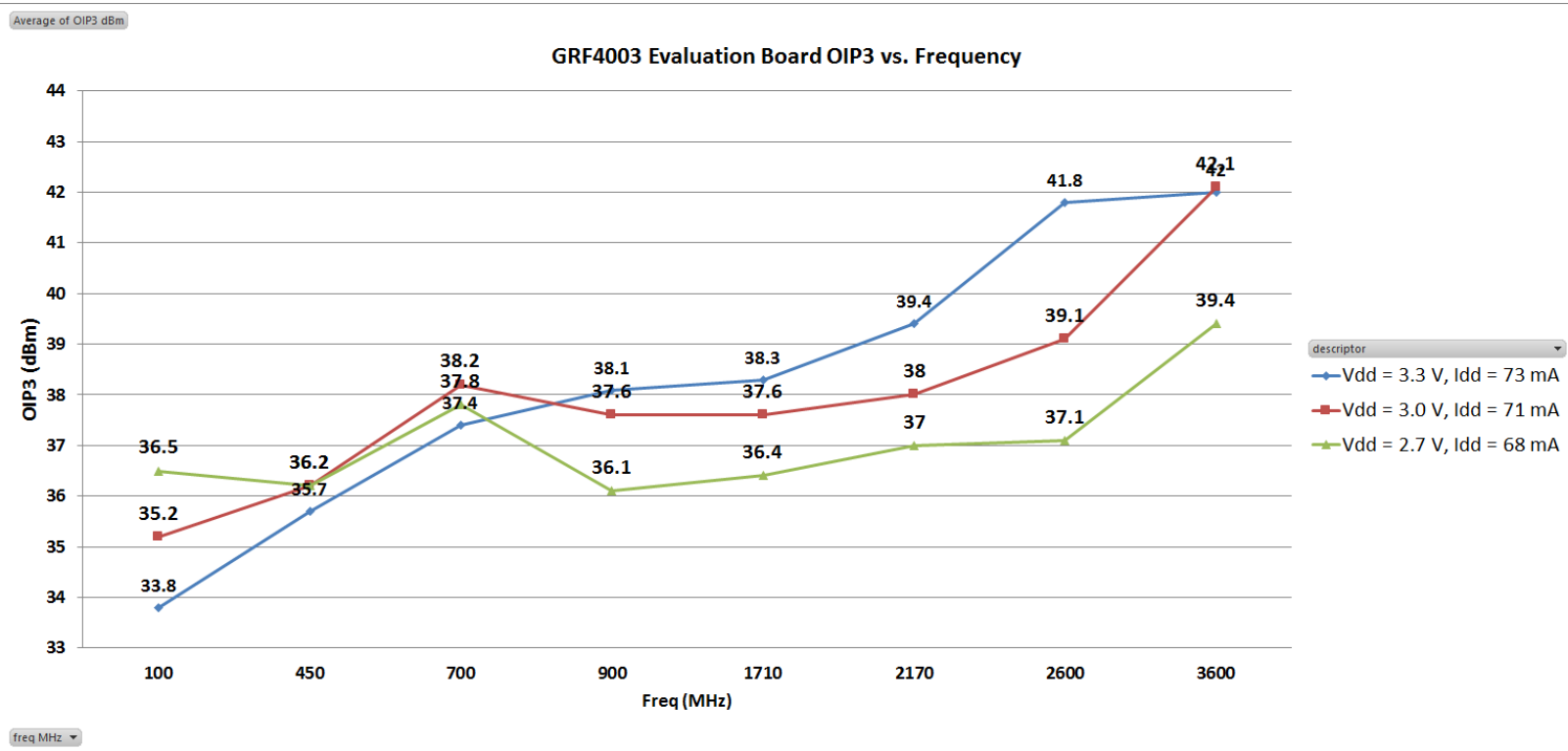




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OIP3:

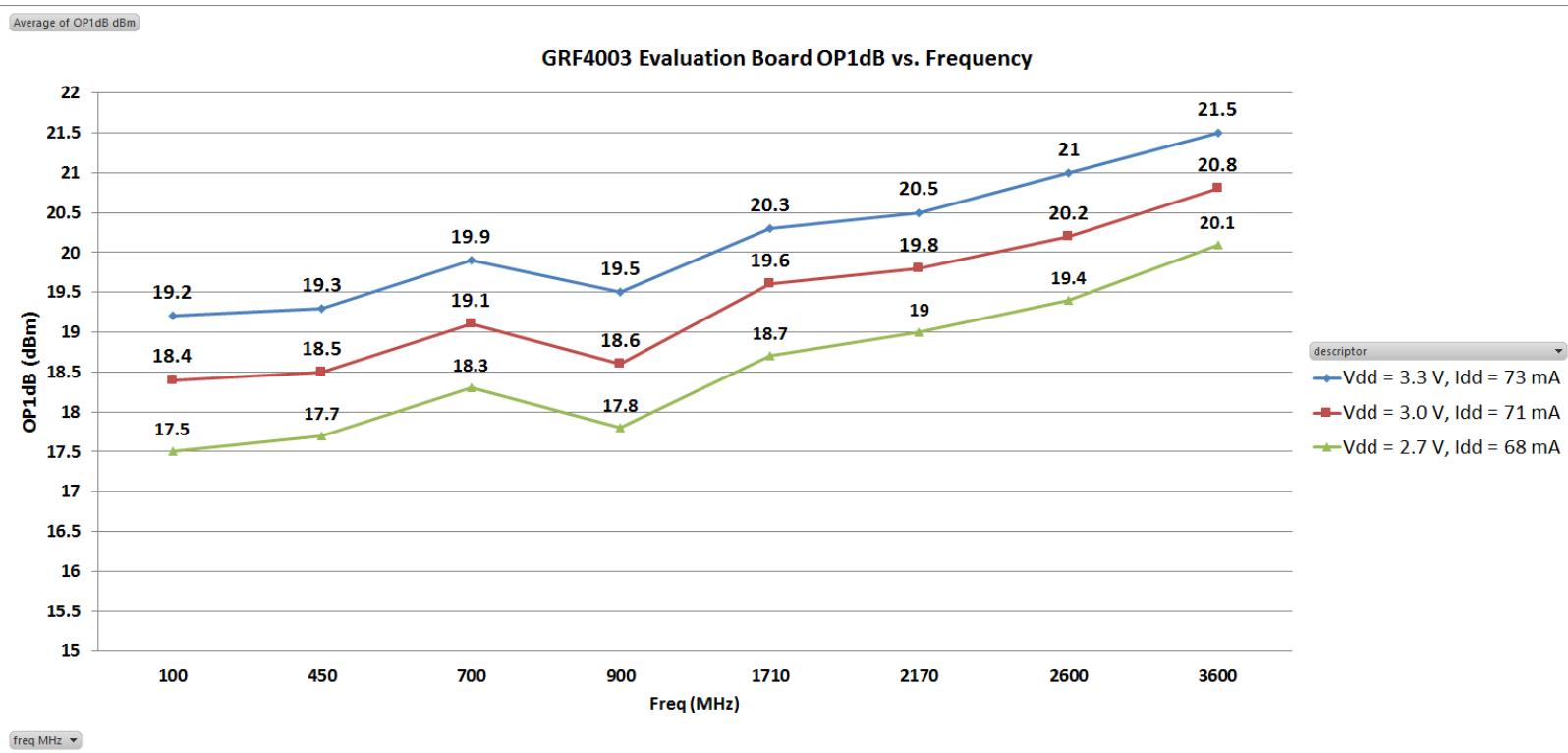




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OP1dB:

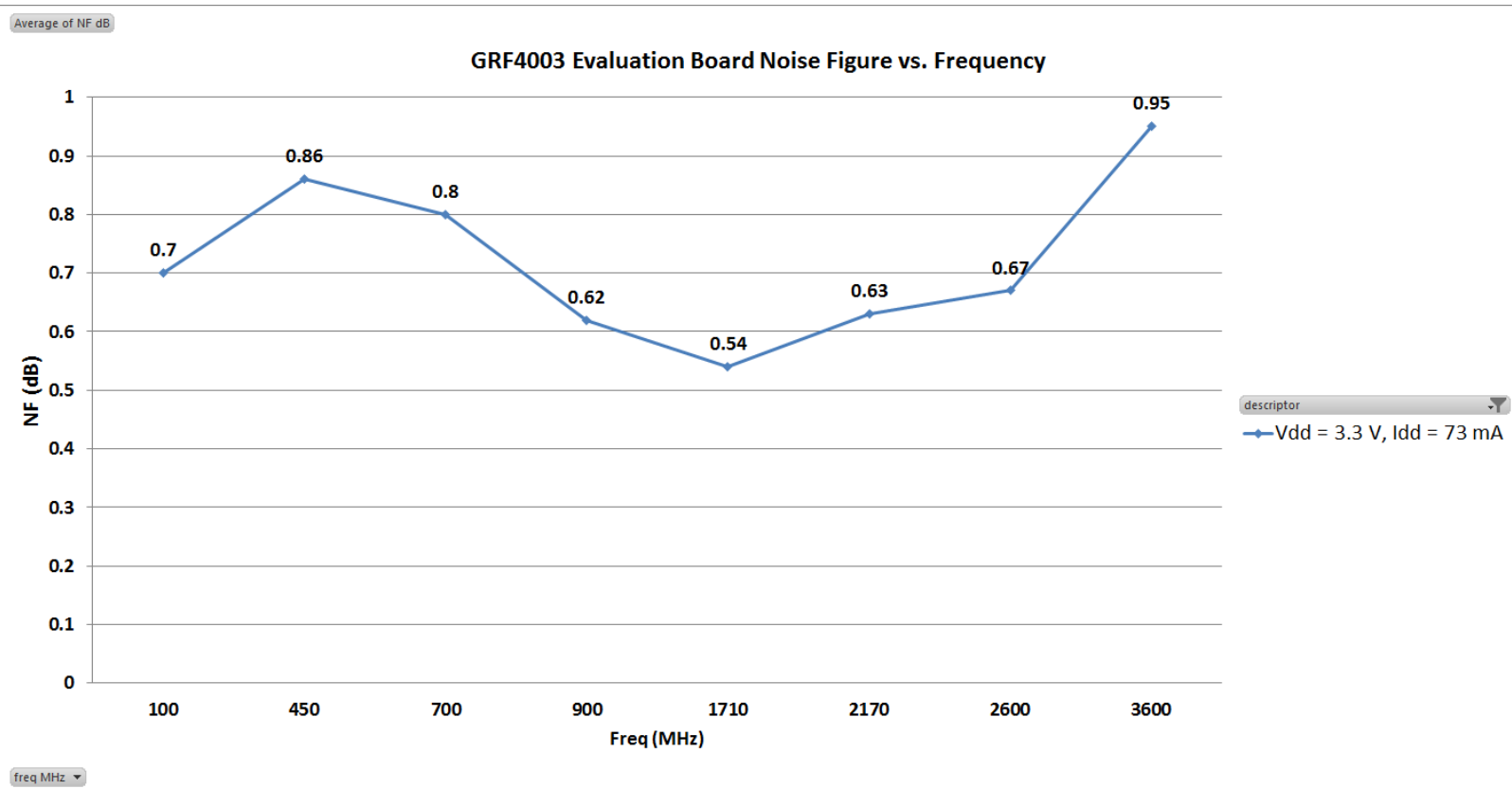




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Noise Figure:





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Tabular data summary:

| descriptor | freq MHz | Vdd V | Idd mA | Gain dB | IIP3 dBm | OIP3 dBm | IP1dB dBm | OP1dB dBm | NF dB |
|--------------------------|----------|-------|--------|---------|----------|----------|-----------|-----------|-------|
| Vdd = 2.7 V, Idd = 68 mA | 100 | 2.7 | 68 | 26.5 | 10 | 36.5 | -7.9 | 17.5 | 0.7 |
| Vdd = 2.7 V, Idd = 68 mA | 450 | 2.7 | 68 | 24.8 | 11.3 | 36.2 | -6 | 17.7 | 0.86 |
| Vdd = 2.7 V, Idd = 68 mA | 700 | 2.7 | 68 | 22.5 | 15.3 | 37.8 | -3.1 | 18.3 | 0.8 |
| Vdd = 2.7 V, Idd = 68 mA | 900 | 2.7 | 68 | 21.3 | 14.8 | 36.1 | -2.5 | 17.8 | 0.62 |
| Vdd = 2.7 V, Idd = 68 mA | 1710 | 2.7 | 68 | 16.7 | 19.7 | 36.4 | 3 | 18.7 | 0.54 |
| Vdd = 2.7 V, Idd = 68 mA | 2170 | 2.7 | 68 | 14.5 | 22.4 | 37 | 5.4 | 19 | 0.63 |
| Vdd = 2.7 V, Idd = 68 mA | 2600 | 2.7 | 68 | 12.8 | 24.3 | 37.1 | 7.6 | 19.4 | 0.67 |
| Vdd = 2.7 V, Idd = 68 mA | 3600 | 2.7 | 68 | 9.9 | 29.5 | 39.4 | 11.3 | 20.1 | 0.95 |
| Vdd = 3.0 V, Idd = 71 mA | 100 | 3 | 71 | 26.6 | 8.7 | 35.2 | -7.1 | 18.4 | 0.7 |
| Vdd = 3.0 V, Idd = 71 mA | 450 | 3 | 71 | 24.9 | 11.3 | 36.2 | -5.4 | 18.5 | 0.86 |
| Vdd = 3.0 V, Idd = 71 mA | 700 | 3 | 71 | 22.5 | 15.6 | 38.2 | -2.4 | 19.1 | 0.8 |
| Vdd = 3.0 V, Idd = 71 mA | 900 | 3 | 71 | 21.3 | 16.3 | 37.6 | -1.7 | 18.6 | 0.62 |
| Vdd = 3.0 V, Idd = 71 mA | 1710 | 3 | 71 | 16.8 | 20.8 | 37.6 | 4 | 19.6 | 0.54 |
| Vdd = 3.0 V, Idd = 71 mA | 2170 | 3 | 71 | 14.6 | 23.5 | 38 | 6.1 | 19.8 | 0.63 |
| Vdd = 3.0 V, Idd = 71 mA | 2600 | 3 | 71 | 12.8 | 26.2 | 39.1 | 8.4 | 20.2 | 0.67 |
| Vdd = 3.0 V, Idd = 71 mA | 3600 | 3 | 71 | 10 | 32.2 | 42.1 | 11.9 | 20.8 | 0.95 |
| Vdd = 3.3 V, Idd = 73 mA | 100 | 3.3 | 73 | 26.6 | 7.2 | 33.8 | -6.4 | 19.2 | 0.7 |
| Vdd = 3.3 V, Idd = 73 mA | 450 | 3.3 | 73 | 25 | 10.7 | 35.7 | -4.7 | 19.3 | 0.86 |
| Vdd = 3.3 V, Idd = 73 mA | 700 | 3.3 | 73 | 22.6 | 14.8 | 37.4 | -1.7 | 19.9 | 0.8 |
| Vdd = 3.3 V, Idd = 73 mA | 900 | 3.3 | 73 | 21.4 | 16.7 | 38.1 | -0.9 | 19.5 | 0.62 |
| Vdd = 3.3 V, Idd = 73 mA | 1710 | 3.3 | 73 | 16.8 | 21.6 | 38.3 | 4.5 | 20.3 | 0.54 |
| Vdd = 3.3 V, Idd = 73 mA | 2170 | 3.3 | 73 | 14.6 | 24.8 | 39.4 | 6.9 | 20.5 | 0.63 |
| Vdd = 3.3 V, Idd = 73 mA | 2600 | 3.3 | 73 | 12.9 | 29.4 | 41.8 | 9.1 | 21 | 0.67 |
| Vdd = 3.3 V, Idd = 73 mA | 3600 | 3.3 | 73 | 10 | 32 | 42 | 12.6 | 21.5 | 0.95 |



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GRF4003 design and associated evaluation board configurations provide the system/radio designer convenient options in extracting performance to accommodate specific applications, one of which outlined here. The flexibility to do so makes it an excellent candidate across different designs, as well as that within multiple slots on the same platform.

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